1. PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Additional voltage value for PWR_1 rail V0.1
DATE:	April 26, 2016
AFFECTED DOCUMENT:	PCIe BGA SSD 11.5x13 ECR
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Part I

1.1. Summary of the Functional Changes

This proposal adds an additional voltage value to the PWR_1 rail in the PCIe BGA SSD 11.5x13 ECR.

Table 3 of section 3.4 in the document “PCIe BGA SSD 11.5x13 ECR”, defines the PWR_1 signal as a 3.3V source. This is changed to now also include a 2.5V rail.

1.2. Benefits as a Result of the Changes

Similar to the multiple voltage options defined for PWR_2 and PWR_3 rails, supporting 2.5V in addition to 3.3V for the PWR_1 rail provides flexibility. It also accommodates the trend of a move to the lower NAND array power supply voltage. Finally it helps simplify the design by removing the need for additional regulators inside the BGA package.

1.3. Assessment of the Impact

This change has no impact on the 11.5 mm x13 mm form factor or any of the other BGA form factors. However the change does require updates to parameters in Section 4.3: “Electrical Requirements for BGA SSDs”, relevant to the new 2.5V power rail. In addition, it requires clarification that M.2 modules will continue to rely on 3.3V rail support.

1.4. Analysis of the Hardware Implications

New electrical requirements defined for the 2.5V power rail.

1.5. Analysis of the Software Implications

N/A.

1.6. Analysis of the C&I Test Implications

N/A.

Part II

Detailed Description of the change

Black text is taken from the "PCIe_BGASSD_11.5x13_ECR". Added text is red.

3.4 BGA SSD Interface Signals

Table 1. BGA SSD System Interface Signal Table for Types 1620, 2024, 2228, 2828

Category	Signal Name	I/O	Function	IO Voltage
Power and Grounds	PWR_1[1] (8 pins)	I	+3.3 V or +2.5V source	
	PWR_2[1] (12 pins)	I	+1.8 V or +1.2 V[1] source	
	PWR_3[1] (12 pins)	I	+1.2 V, +1.1 V[1], or +0.9 V[1] source	
	GND (106 pins)		Return current path	0 V

4.3 Electrical Requirements for BGA SSDs

4.3.3 BGA SSD Power Ramp Timing

The power ramp timing is defined as the time the power rail needs to ramp to a valid voltage (shown in **Error! Reference source not found.**). This timing is recommended for power-on only.

Table 2. Power Ramp Timing

Supply Voltage	Max*
3.3 V	35 ms
2.5V	30 ms
1.8 V	25 ms
1.2 V	20 ms
1.1 V	20 ms
0.9 V	20 ms

4.3.4 BGA SSD Power Rail Slew Rate

The maximum power rail slew rate is shown in **Error! Reference source not found.**. These values are only defined for ESD protection purpose. They are not meant for inrush current control.

Table 3. Power Rail Slew Rate

Symbol	Parameter	Max	Condition
$T_{SLEW\_3.3}$	Voltage slew rate of the 3.3 V power rail	100 kV/s	No Load
$T_{SLEW\_2.5}$	Voltage slew rate of the 2.5 V power rail	100 kV/s	No Load
$T_{SLEW\_1.8}$	Voltage slew rate of the 1.8 V power rail	100 kV/s	No Load
$T_{SLEW\_1.2}$	Voltage slew rate of the 1.2 V power rail	100 kV/s	No Load
$T_{SLEW\_1.1}$	Voltage slew rate of the 1.1 V power rail	100 kV/s	No Load
$T_{SLEW\_0.9}$	Voltage slew rate of the 0.9 V power rail	100 kV/s	No Load

4.3.5 BGA SSD Power Rail Parameters

All supply voltages and tolerances referenced for BGA SSD devices in this specification are considered to be measured at the component ball or pin. Supply tolerances are assumed to incorporate any superposition of AC, DC and system transient effects measured at the component ball or pin.

Table 7 describes the characteristics of the regulated power rails for a BGA SSDs.

Table 7. Regulated Power Rail Parameters for BGA SSD Types

Nominal Voltage	Voltage Range	Platform Rail Type
+3.3 V	2.8 V to 3.6 V	Always On
+2.5V	2.45 V to 2.75 V	Always On
+1.8 V	1.7 V to 1.9 V	Always On
+1.2 V	1.14 V to 1.26 V	Always On
+1.1 V	1.06 V to 1.17 V	Always On
+0.9 V	0.86 V to 0.98 V	Always On

4.4 Power

The M.2 module utilizes a single regulated power rail of 3.3 V provided by the platform. The 2.5V power rail is relevant solely for BGA SSD. In some pinout variants, there is a dedicated VIO supply pin called VIO1.8V that is intended to only bias the I/O circuitry of the module. The main 3.3 V and the VIO voltage rail sources on the platform should always be on and available during the system's stand-by/suspend state to support the wake event processing on the communications card. Some NICs may require host (driver) intervention after a power-on.

The number of 3.3 V pins for any given pinout is determined by the maximum required instantaneous current typical of the solutions associated with each type of socket and the M.2 connector current handling capability per pin. The M.2 connector pin is defined as needing to support 500 mA/pin continuous. This yields the required number of power rail pins per pinout.

- Type 1630, intended for Socket 1, has two power pins allocated in the pinouts that supports up to 1 A continuous.
- Types 2230 and 3030, intended for Socket 1, have four power pins in their pinouts and can support up to 2 A continuous.
- The Socket 2 board types have five power pins in their pinouts and can support up to 2.5 A continuous.
- The Socket 3 board types, with a single Module Key, have nine power pins but can support up to 2.5 A continuous.
- The four extra power pins enable reduced IR drop for these devices.